ERS

RADIANODE ENGINEERING READINESS SERIES

ERS-2026-003

Engineering Readiness Assessment

Why Carrier-Board Module-Current Measurements Can Be Misleading

Off-state current attribution at the supply header of two off-the-shelf cellular carrier boards

INDEPENDENT ENGINEERING VALIDATION

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Executive Summary

A current measurement at a cellular carrier board's supply header records the current entering the board through that point. Where the module shares this supply path with other loads, the reading includes their consumption. Additional supply inputs can complicate the measurement and must be accounted for before the result is attributed to the module.

This assessment examined two off-the-shelf carrier boards from different vendors, carrying modules from two manufacturers, with the same instrument.

The **BG95-M3 on the DIP40CORE-A breakout** drew **1.539 mA** over a 30-minute capture, about **118 times** Quectel's published BG95-series power-off leakage figure of 12.99 µA (Quectel publishes no separate LA-variant figure). The module's off state was checked using its STATUS and VDD-EXT outputs, and the measurement reproduced the earlier 1.53 mA result within 0.6 %.

The **SIM7080G on the Waveshare Cat-M/NB-IoT HAT**, reported in ERS-2026-002 at 2.06 mA, was re-measured at 3,800 mV. After a PWRKEY power-down the header drew **1.886 mA**, at least **125 times** SIMCom's published maximum power-off current of 15 µA and within 0.5 % of its level before the module was first switched on.

Module-level current could not be isolated on either board. On the SIM7080G board the schematic places an always-on power LED on the shared VBAT net, and the available evidence points to board-level consumption. On the BG95-M3 board, two resistive paths on the schematic account for an estimated 0.3 to 0.4 mA, and the bench showed that the on-board regulator's unconnected input is back-powered from the supply rail to 3.33 V. The current through that path was not measured, so the remaining current has not been accounted for.

The report defines a procedure for checking supply topology, confirming module state independently of the current reading, and comparing the measurement with the matching manufacturer figure. Sleep and Power Saving Mode (PSM) current were not measured; the next step is a DIP40CORE-A header measurement in network-confirmed PSM.

ENGINEERING DECISION

Can a cellular module's low-current behaviour be measured at the supply header of an off-the-shelf carrier board, and how does an engineer find out before trusting the number?

Investigation scope

ITEM	DESCRIPTION
Engineering asset	Supply-header current access on two cellular-module carrier boards
Engineering objective	Determine whether supply-header current can be attributed to the module alone, and define a procedure for assessing attribution on carrier boards
Boards evaluated	Waveshare SIM7080G Cat-M/NB-IoT HAT (SIMCom SIM7080G) · DIP40CORE-A breakout, silkscreen "BG95 V1.1" (Quectel BG95-M3, SKU BG95M3LA-64-SGNS, firmware BG95M3LAR02A03)
Primary instrument	Nordic Power Profiler Kit II, serial D439F20BA129, Power Profiler v4.4.1, 100 kS/s
Comparators	Module manufacturers' hardware design documents, cited by version and table
Constraint	No hardware modification. No trace cuts, no component lifts
RVP	Radianode's method linking engineering question, expected behaviour, evidence and decision, so conclusions stay traceable to evidence

TERMINOLOGY *Off state*: module powered down with its supply rail energized. *Header current*: current measured at the board's supply header pin. *Attribution*: assigning measured current to the module rather than to the board as a whole.

ENGINEERING PROCESS

RVP · Radianode Validation Process

STAGE	DEFINITION	APPLICATION IN ERS-2026-003
RVP-01 Assess	Define the problem: requirements, architecture, constraints, scope	Identified the supply header as the only unmodified access point on each board; established supply topology from vendor documentation
RVP-02 Simulate	Engineering analysis of expected behaviour, by numerical simulation or by analysis from published specifications	Derived the expected module-only off-state current from the manufacturers' specifications and set the measurement criteria before the bench session
RVP-03 Validate	Verify assumptions against objective evidence	Re-measured the DIP40CORE-A against pre-set criteria with raw data retained; confirmed module state by two signals independent of current; tested for UART back-feed by a recorded module-side disconnection; tested a candidate board-level path; re-measured the Waveshare HAT at a recorded supply condition, with the module started and powered down by PWRKEY
RVP-04 Decide	Evaluate evidence against requirements and residual uncertainty	Established the attribution level each board supports and the conditions under which a header reading may be read as module current

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Measurement Basis

ENGINEERING QUESTION

Is the instrument fit to make the readings this assessment depends on?

The available instrument checks and their reference limitations are summarised below.

CHECK	RESULT	REFERENCE QUALITY	SOURCE
PPK2 source-meter mode, 18 mA load	0.58 % deviation	Calculated reference: 3.992 V ÷ 220 Ω = 18.145 mA, using the nominal 220 Ω resistance (±5 %). The load measured 217.5 Ω on the uncalibrated MS8268	ERS-2026-002 §01
PPK2 ampere-meter mode, same load	0.22 % deviation	Against the 18.18 mA theoretical value stated in ERS-2026-002	ERS-2026-002 §01
PPK2 ampere-meter mode vs HP 6611C readback, time-matched	−0.02 % at 2.5 V / ~470 mA	Calibrated supply (5 Dec 2025)	Radianode instrument cross-check, 2026

Note. The 0.58 % deviation compares the displayed 18.25 mA mean with the unrounded 18.145 mA reference. ERS-2026-002 reported 0.55 % using the rounded 18.15 mA reference.

Traceability caveat. Only the HP 6611C check is against a calibrated reference, and it was made in ampere-meter mode at about 470 mA. The 18 mA checks rest on a nominal-value calculation for a ±5 % resistor, not on a calibrated reference. The off-state readings on both boards were taken in source-meter mode at 1.5 to 1.9 mA: the mode was checked only at 18 mA, and no check point exists in that range. These operating points remain unvalidated. An error at the percent level, however, would not explain a discrepancy of approximately two orders of magnitude.

The BG95-M3 readings in §03 were taken in **source-meter mode at 3,800 mV, 100 kS/s**, the supply condition at which Quectel specifies its figures. In the 14 October session the mode is recorded in the application log ("Mode: Source meter", 20:20:59) and is shown on screen during the run 2 recording (Figure 1a). For the September 2026 captures it was established from the display: in the PPK2 application a supply-voltage setting is shown only in source-meter mode, and a reference view logged as ampere-meter mode shows the opposite selector highlighted and no voltage setting (Figure 1b, c). VBAT at the module pin read 3.838 V on the uncalibrated MS8268 during the session; the set point, not that reading, is stated as the supply condition.

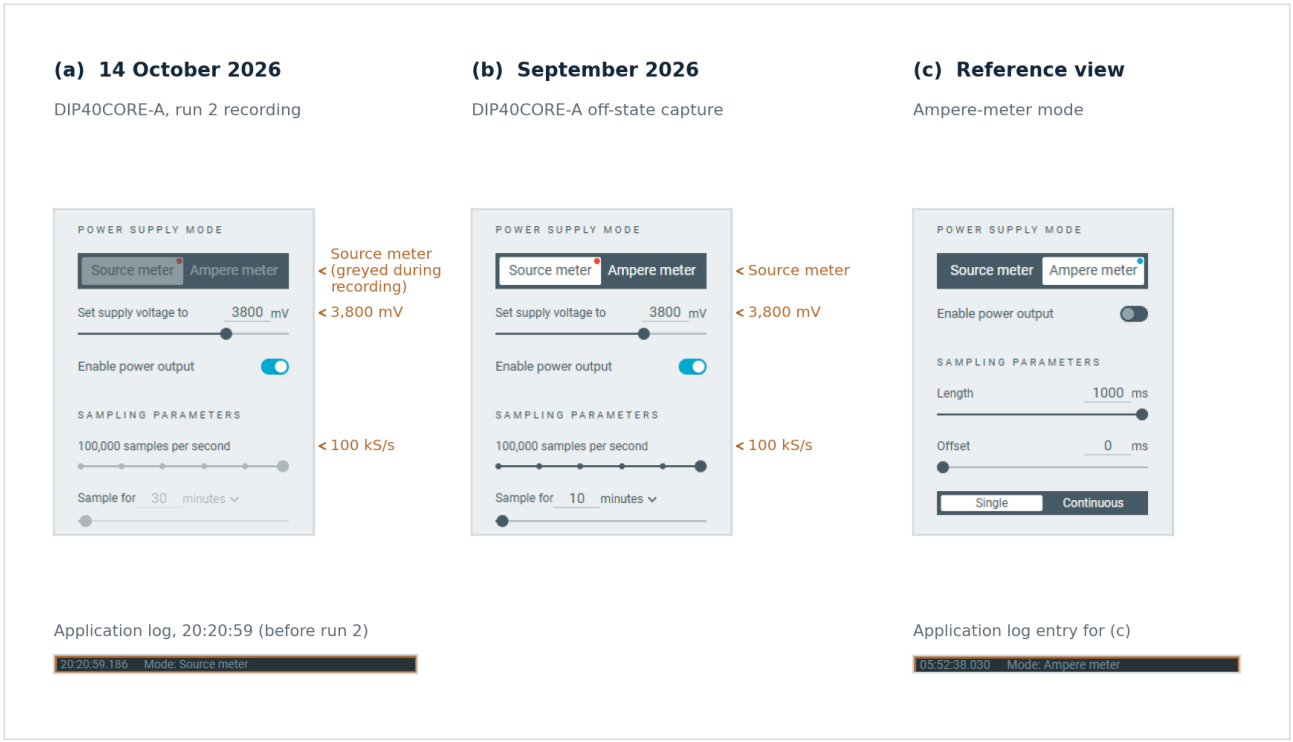


FIGURE 1 *PPK2 operating-mode evidence.* (a) Settings displayed during the 14 October 2026 DIP40CORE-A run 2 recording: source-meter mode, a 3,800 mV supply setting and a 100 kS/s sampling rate; the selector is greyed during recording. A separate application-log entry at 20:20:59, about 12 minutes before the run 2 recording began (same PC clock), records source-meter mode; no later mode entry appears before run 2. (b) September 2026 DIP40CORE-A capture showing the same settings. (c) Reference view showing ampere-meter mode, in which the supply-voltage setting is not displayed. The September capture's operating mode was inferred from the displayed controls.

Range caveat. The off-state readings sit between 1.5 and 1.9 mA. PPK2 range-transition behaviour has not been characterized on this bench. The raw off-state data contain short events reading 0.2 µA (§3.3); the same signature occurs once in Waveshare HAT recording 1. Whether these are range-switching artefacts is not established. They bear on fine trace structure, not on a two-order-of-magnitude discrepancy.

■ **Engineering Finding** · The checks showed deviations below 1 % at their respective test points, one of which was checked against a calibrated reference. However, the source-meter operating point used for the off-state measurements was not directly validated. An error of approximately two orders of magnitude would be required to explain the observed discrepancies on instrumental grounds alone.

02

SIM7080G on the Waveshare HAT

ENGINEERING QUESTION

With the module powered down by PWRKEY, what does the supply header draw, and how does that compare with the module's own specification?

ERS-2026-002 §04 reported this board's off-state current from a 26 August 2026 capture whose supply voltage and instrument mode were not recorded. The board was re-measured on 15 October 2026 in two 5-minute recordings at a recorded supply condition. In each, the module stayed off after the supply was applied, was started with PWRKEY, and was then powered down with PWRKEY.

OBSERVATION	RESULT	SOURCE
Access point	Single breakout header; no test point adjacent to the module	ERS-2026-002 §04
Header topology	Header H1 pin 1 is the VBAT net itself, shared with module VBAT (pins 34, 35), the PWR LED (R12, 1 kΩ), regulator U2 (RT9193-33, EN tied to VIN) and the cathode of D1 (B5819WS). With the header as sole source, every consumer on that net draws through it	Waveshare HAT schematic; ERS-2026-002 §04 recorded this as unresolved
Module state	Off when the supply was applied; started and then powered down with PWRKEY in each recording (Figure 2a). The STA LED, driven by the module's STATUS output, was dark while the module was off and lit while it was on (Figure 4c, d)	Recordings and photographs, 15 Oct 2026; operator record of PWRKEY timing
Supply configuration	USB connector empty, HAT not mounted on a Pi, jumper P2 bridging 5V to VCC, PWR-to-P7 open; no antenna; SIM fitted. U1 therefore had no input, and U2's 3V3 output fed no drawn load. The 26 August photograph shows the same supply configuration, with the PWR-to-P7 jumper fitted	Waveshare HAT schematic; photographs, 15 Oct and 26 Aug 2026 (Figure 4)
Recording conditions	15 October: two 300.00 s recordings, source-meter mode, 3,800 mV, 100 kS/s, raw data retained. 26 August: 10.00 s; supply voltage and instrument mode not recorded	Raw capture files; instrument screenshots, 15 Oct 2026
Off-state header current, 15 October	Recording 2: 1.894 mA over 211.5 s before power-on; **1.886 mA** over 19.7 s after power-down. Recording 1: 1.882 mA over 79.2 s before; 1.872 mA over 55.2 s after. Means exclude 1 s either side of each transition	Raw sample data, 15 Oct 2026
On-state header current, 15 October	Recording 2: 23.6 mA mean over 66.8 s; peaks to 221 mA	Raw sample data, 15 Oct 2026
Off-state header current, 26 August	2.06 mA average, 2.15 mA maximum, over 10.00 s. Raw capture data: 2.062 mA mean, 2.148 mA max, 1,000,001 samples	ERS-2026-002 §04; raw capture file
Module manufacturer power-off figure	**15 µA, maximum** (no typical value published)	SIMCom HD V1.04 Table 6; same value in V1.03 Table 6 and V1.05 Table 7

OBSERVATION	RESULT	SOURCE
Module manufacturer PSM figure	3 µA typical	SIMCom HD V1.04, Tables 6 and 33
Board vendor PSM figure	3.2 µA	Waveshare HAT product specification (as used in ERS-2026-002, TB-2026-001)

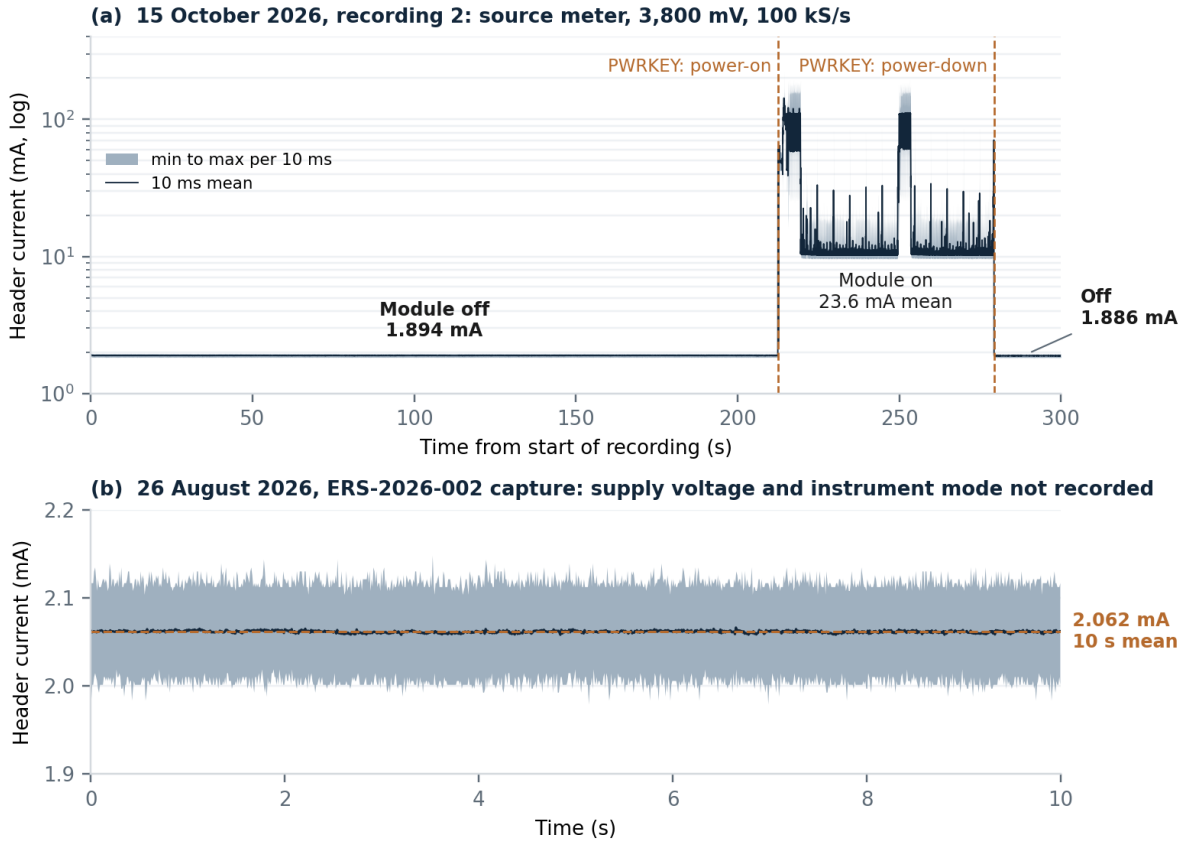


FIGURE 2 *Waveshare HAT header current.* (a) 15 October 2026, recording 2: the module off after the supply was applied, started with PWRKEY at 212.49 s and powered down with PWRKEY at 279.29 s; 10 ms means and range on a logarithmic scale. (b) The 26 August 2026 capture reported in ERS-2026-002. Both plotted from the raw sample data.

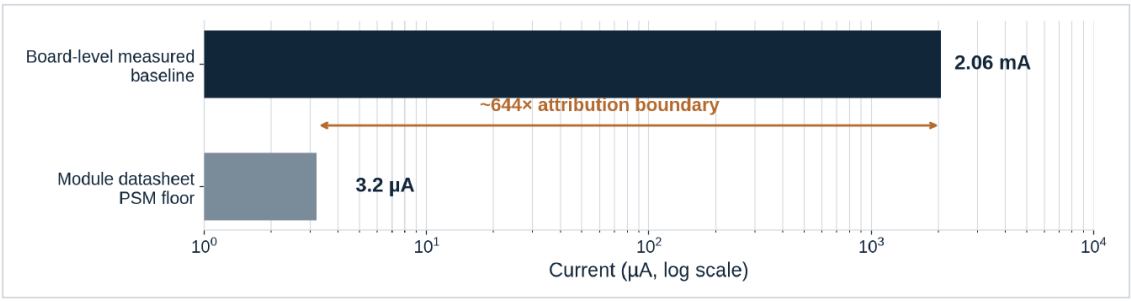
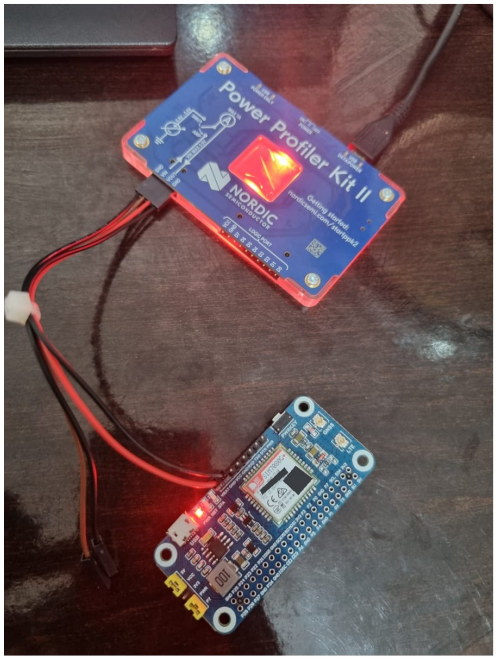
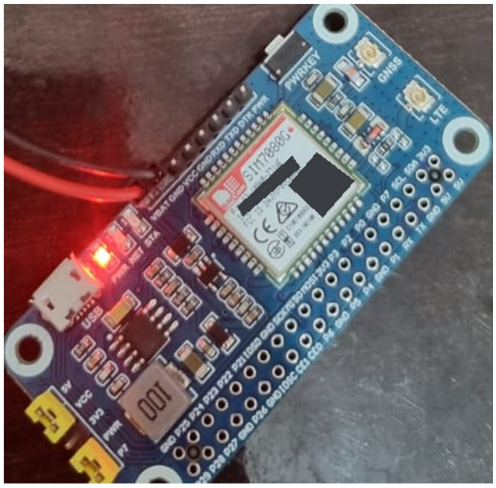


FIGURE 3 *Previously published comparison of Waveshare HAT header current with the published low-power current figure.* Reproduced from ERS-2026-002, Figure 4. The 3.2 µA value is the Waveshare board-vendor figure; SIMCom publishes a typical module PSM current of 3 µA.

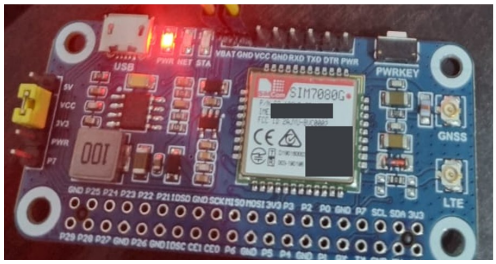
(a) Attachment, 26 August 2026
PPK2 output connected to the HAT supply header



(b) Detail of (a)
USB connector empty; P2 jumper 5V–VCC; PWR LED lit



(c) 15 October 2026, module off
PWR LED lit; STA LED dark; PWR–P7 open



(d) 15 October 2026, module on
PWR LED and STA LED lit

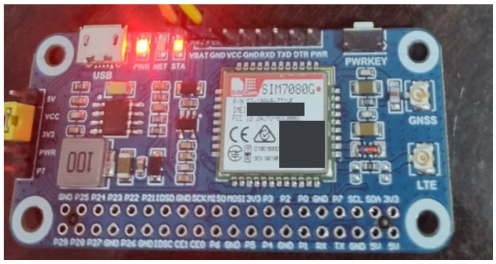
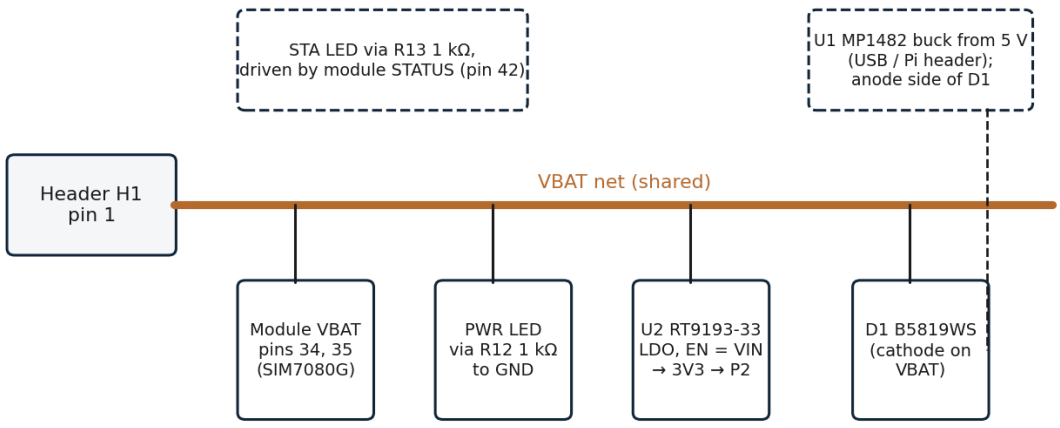


FIGURE 4 *Waveshare HAT measurement configuration.* (a) PPK2 connected to the HAT supply header on 26 August 2026. (b) Close-up showing the empty USB connector, P2 jumper bridging 5V to VCC, and illuminated PWR LED. (c) 15 October 2026, module off: PWR LED lit, STA LED dark, PWR-to-P7 open. (d) 15 October 2026, module on: STA LED lit. The module's IMEI and QR code are redacted.



Redrawn by Radianode from the Waveshare SIM7080X Cat-M/NB-IoT HAT schematic. Simplified; not a reproduction.

FIGURE 5 *Waveshare HAT VBAT net, redrawn.* Simplified net diagram drawn by Radianode from the Waveshare SIM7080X Cat-M/NB-IoT HAT schematic (Altium, 2020-01-19). The schematic's title matches the board's underside silkscreen ("SIM7080X Cat-M/NB-IoT HAT"); no revision code is marked on the board, so revision correspondence is not confirmed.

ENGINEERING INTERPRETATION

In both recordings, the header current after a PWRKEY power-down returned to within 0.6 % of its level before the module was first switched on: 1.886 against 1.894 mA, and 1.872 against 1.882 mA. On this board, the off-state reading is the same whether the module has never been started or has been powered down. Against SIMCom's 15 µA power-off maximum, 1.886 mA is at least 125 times higher (a lower bound, because the comparator is a maximum and no typical value is published).

The 26 August reading, 2.06 mA, is about 9 % above the October level. Its supply voltage was not recorded, so the difference cannot be assigned. A higher supply voltage would raise the current in the LED branch described below; this has not been tested.

In recording 1, the current fell to about 2 mA for 47 ms at 217.7 s while the module was on, then repeated the power-on pattern. The cause was not identified; the off-state values, taken before power-on and after power-down, are unaffected.

Identified board-level consumers. The HAT schematic places three consumers on the VBAT net besides the module: the PWR LED through a 1 kΩ resistor, which is always on whenever VBAT is present and was recorded lit; regulator U2, whose enable is tied to its input, and whose output load depends on jumper P2: with P2 bridging 5V to VCC, as photographed (Figure 4), U2's 3V3 output feeds no drawn load and only its quiescent current remains; and the reverse leakage of Schottky D1. At the 3.8 V supply, with an LED forward voltage near 2 V, the 1 kΩ LED branch alone would draw about 1.8 mA, close to the whole off-state reading. That is an estimate, not a measurement: neither the forward voltage nor U2's quiescent current has been measured on this board. It is testable without modification by reading the voltage across R12 (I = V / 1 kΩ).

Limits of the Waveshare HAT evidence. (1) The module state rests on PWRKEY control and the STA LED. STATUS was not read with a meter, and SIMCom specifies its 1.8 V-domain output high level at only 1.35 to 1.8 V (V1.04, Table 30), close to a red LED's forward voltage; the LED was nonetheless photographed lit with the module on. (2) The schematic revision is not tied to this board by a revision marking. (3) The off-state windows, 19.7 s to 211.5 s, are shorter than the 10 minutes set in §05, step 5. Within each window, the means of the first and second halves agree within 1.3 µA. (4) SIMCom publishes its power-off figure without test conditions; PWRKEY is one of its documented power-off methods (HD V1.04, §3.2.2). (5) The 26 August capture's supply voltage and instrument mode remain unrecorded, and that day's configuration differed in the PWR-to-P7 jumper.

✗ **Engineering Finding** · Module-level current attribution is **not achieved** at the header of this board. With the module powered down by PWRKEY and the supply recorded at 3.8 V, the header current is at least 125 times the module's power-off maximum, and the available evidence points to board-level consumption.

03

BG95-M3 on the DIP40CORE-A Breakout

ENGINEERING QUESTION

With the module confirmed off by signals independent of the current reading, what does the supply header draw, and can the excess be attributed?

The initial September 2026 measurements of the DIP40CORE-A, made during Radianode's Cat-M1 measurement campaign, are documented by screenshots only. A **dedicated measurement session on 14 October 2026** was then conducted against predefined acceptance criteria, with raw data retained. The session produced three recordings, referred to below as run 1 (70 s, module on), run 2 (30 min: on state, power-down, off state) and run 3 (30 min, off state, hands off), and a 5-minute UART disconnection test. The figures below are from the re-measurement unless marked otherwise.

3.1 Identity and topology

ITEM	FINDING	SOURCE
Module	Quectel BG95-M3, SKU **BG95M3LA-64-SGNS** (LA variant), read from the module marking (Figure 6). `ATI` returns "Quectel / BG95-M3 / Revision: BG95M3LAR02A03"	Marking photograph (Figure 6); AT transcript, 14 Oct 2026
Board	DIP40CORE-A, silkscreen "DIP40CORE-A BG95 V1.1". No reference designators on either face	Board inspection, 14 Oct 2026
Module supply pins	Two pairs: VBAT_BB (32, 33), VBAT_RF (52, 53), both on the board's single VBAT net	Vendor schematic DIP40CORE-A BG95 (20230417)
Board supply net	**Single VBAT net:** header pin 39, U7 (JW5033H) switch node via L3 4.7 µH, U7 feedback divider R26 15 kΩ + R27 3.9 kΩ to ground, D2 LED via R2 10 kΩ, C8 and C9 (100 µF) with C1 to C7, and module VBAT pins 32/33 and 52/53. Q2-switched D3 NET LED via R6 1 kΩ	Vendor schematic DIP40CORE-A BG95 (20230417), supplied by the manufacturer. Module designator on the drawing reads EG915Q-NA; applicability to BG95-M3 per the manufacturer's statement in September 2026 (no written confirmation)
Connections during capture	PPK2 VOUT to header pin 39, GND to pin 40. UART (pins 29, 30) to a Raspberry Pi through a TI TXS0108E level shifter, low side referenced to the module's VDD-EXT (pin 32). **VIN (pin 2) unconnected**. No antenna; no SIM	Figure 8. UART paths confirmed working by the AT exchange (§3.2); other connections, including the open VIN, per the bench wiring record, not confirmed by photograph or continuity check



FIGURE 6 *Quectel BG95-M3 module installed on the DIP40CORE-A breakout.* Photograph taken on 14 October 2026. (a) The module on the breakout; (b) the package marking, enlarged, identifying the LA variant and SKU BG95M3LA-64-SGNS. The unit serial number, IMEI and QR code are redacted.

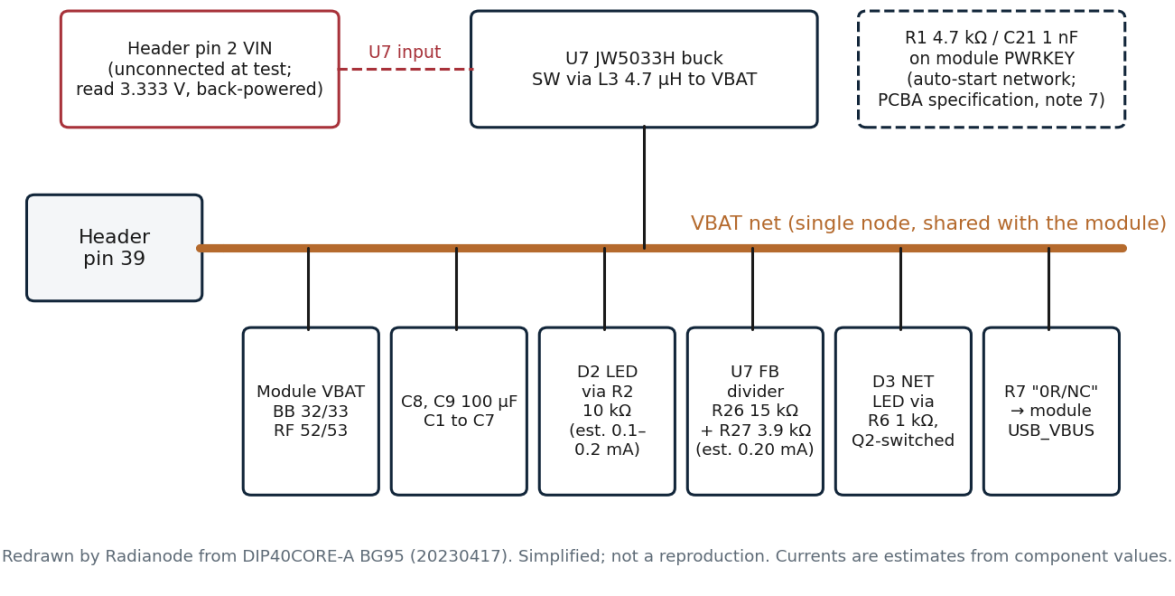


FIGURE 7 *DIP40CORE-A VBAT net, redrawn.* Simplified net diagram drawn by Radianode from the vendor schematic DIP40CORE-A BG95 (20230417), with the VIN reading from this session added.

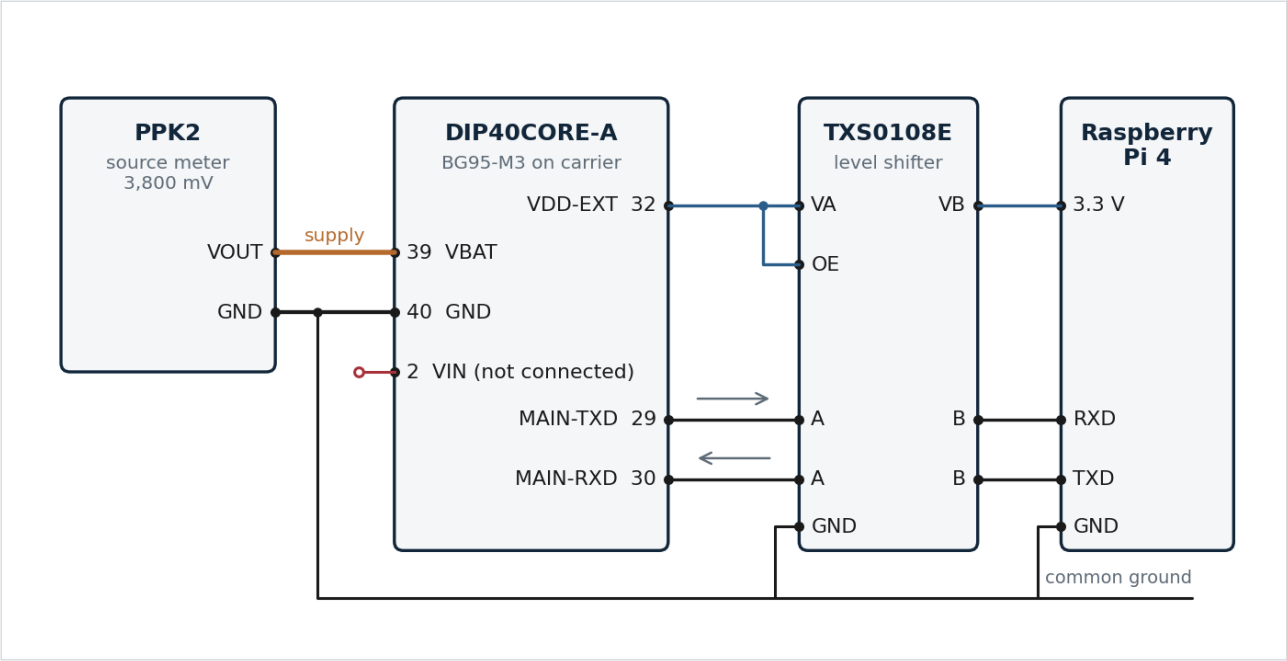


FIGURE 8 *Power and UART connections for the DIP40CORE-A during the 14 October 2026 session.* The PPK2 supplied VBAT at header pin 39, with ground at pin 40; VIN (pin 2) was left unconnected. The TXS0108E level shifter interfaced the module's UART with the Raspberry Pi; its low-voltage reference (VA) was supplied by VDD-EXT, and OE was tied to VA. Successful AT-command exchanges confirmed UART operation. No antenna or SIM was fitted. The diagram is reconstructed from the wiring guide and session record; the setup photographs do not resolve individual connections, and the open VIN was not confirmed by a continuity check.

A shared node does not make pin 39 a valid module measurement point by itself: an ammeter at one tap sees only that tap's current, which equals the module's only if nothing else on the node sources or sinks. With VIN unconnected, no current enters the board except through pin 39, so every consumer on the board, the module included, is inside the measurement. Whether any of them other than the module draws current is the attribution question.

3.2 Establishing the module state

State was established from two module outputs whose only function is to indicate power state, read with a multimeter, and cross-checked against the AT interface. None of them is the current reading.

INDICATOR	MODULE ON	AFTER AT+QPOWD=1	PRE-SET CRITERION
STATUS, header pin 12 (PCBA specification: VOH ≥ 1.35 V, VOL ≤ 0.45 V)	1.8 V	**0.45 V** (two readings)	On ≥ 1.35 V; off ≤ 0.45 V: met, the off reading at the limit
VDD-EXT, header pin 32 (PCBA specification: 1.8 V nominal output)	1.81 V	**0.000 V**	No tolerance published; off reading unambiguous
AT interface	AT → OK; ATI → BG95-M3	OK, then `POWERED DOWN`	
NET LED / PWR LED	Blinking / on	Off / on (PWR LED is on the VBAT net, not the module)	

STATUS and VDD-EXT voltages were recorded manually with an uncalibrated MS8268 multimeter (0.01 V resolution on STATUS). Two STATUS readings were excluded because of probe-contact errors, and a third entry was corrected as a transcription error. The September 2026 record reports 0.03 V for STATUS off; the discrepancy with the 0.45 V obtained here remains unexplained. Because the STATUS off reading sits on the criterion limit, VDD-EXT at 0.000 V is cited alongside it.

Comparison with the September 2026 record. The September 2026 record reports that the `POWERED DOWN` response did not correspond to a drop in current, and that the NET LED reacted identically to a RESET press. In

this session the current fell from 26.2 mA to 1.54 mA at 20:55:08, in the minute the operator recorded sending the command (Figure 11). The earlier behaviour was not reproduced in the October session. The POWERED DOWN response is therefore not treated as independent confirmation of the module state; the assessment relies on STATUS and VDD-EXT alongside the AT-command response. The RESET observation was not re-tested.

3.3 Results

CONDITION	HEADER CURRENT, PIN 39	SOURCE
Module on, no SIM, no antenna	**26.26 mA** mean over the 433 whole seconds before the 20:40:32 event (from 20:33:18 WAT); peaks to 139.6 mA. Second on interval 26.24 mA. September 2026: 25.75 mA over 10 min, peaks 138.01 mA	Saved recording, 14 Oct 2026; September 2026 screenshot
Off after AT+QPOWD=1, 30 min, hands off (run 3)	**1.5388 mA** mean of 180,000,001 samples; σ 36 µA; max 1.81 mA. 10-minute thirds 1.5390, 1.5387, 1.5388 mA. Every 1 s mean within 1.5363 to 1.5440 mA	Raw sample data, 30-minute recording
Off, end of run 2 (8 min after QPOWD)	1.5388 mA (20:55:08 to 21:03:19)	Saved recording, 14 Oct 2026
Off, with UART wires removed at the module side	Segment means 1.5394, 1.5388 and 1.5392 mA, separated by the two handling transients; no 10 s mean departs from the record mean by more than 0.13 %	Raw sample data, UART test
September 2026 off state (for comparison)	1.53 mA over 10:00 min (0.92 C)	September 2026 screenshot

All 14 October readings: source-meter mode, 3,800 mV, 100 kS/s. Pass criterion for the off-state figure, set before the session: the 30-minute mean within ±5 % of 1.53 mA (1.45 to 1.61 mA). **Met: +0.6 %.**

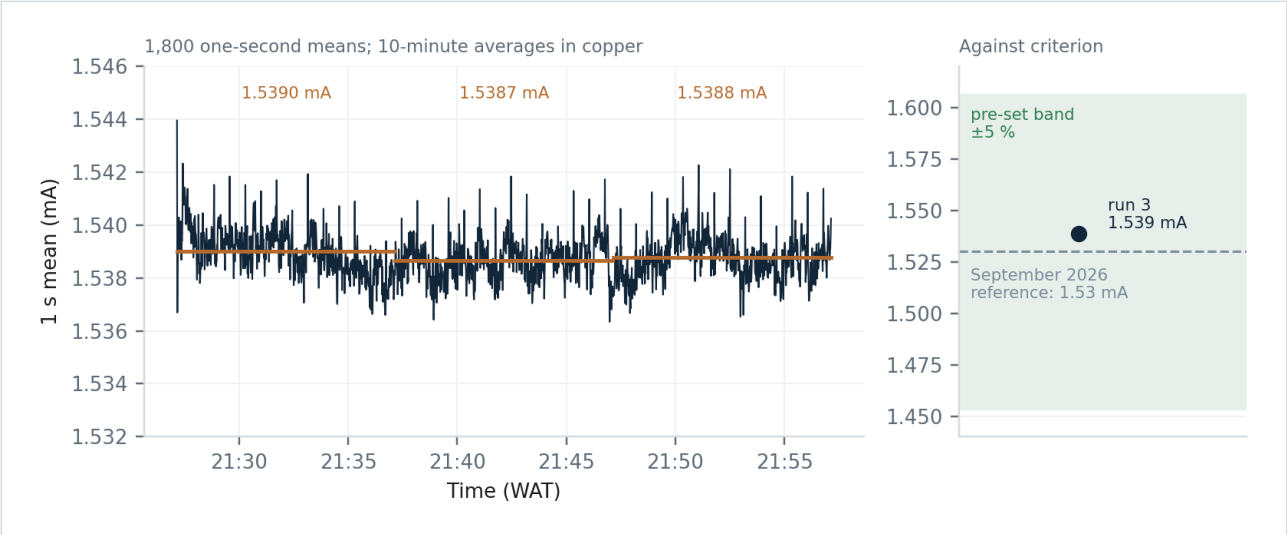


FIGURE 9 *DIP40CORE-A off-state header current over 30 minutes after AT+QPOWD=1 (run 3).* Left: one-second means, with 10-minute averages in copper. Right: the 30-minute mean against the acceptance band set before the session. Computed from the raw sample data.

UART back-feed assessment. With the module off, both UART wires were pulled from the module pins and replaced, during a 5-minute recording (Figure 10). The mean did not change by more than 0.13 %; the pre-set exclusion threshold was 2 %. Two brief transients occurred at 77.6 s (peak 25.9 mA, about 0.6 ms) and 170 s. They are consistent with the UART disconnection and reconnection, but the event timing was recorded only to the nearest minute, so this attribution remains unconfirmed. The conclusion does not depend on it.

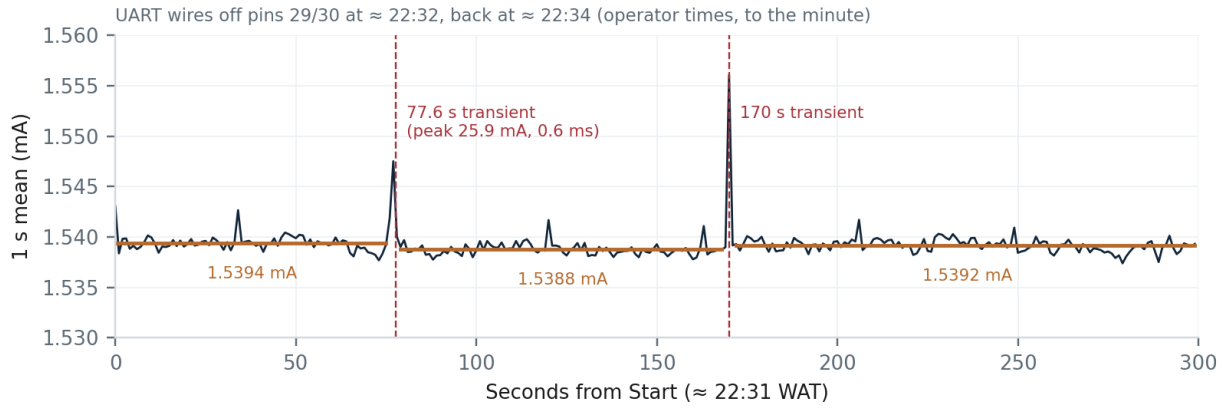


FIGURE 10 *Module-side UART disconnection test, DIP40CORE-A off state.* One-second means over the 5-minute recording; copper lines are the means of the segments between handling transients. Computed from the raw sample data.

High-current tracking. In the on state the header registered peaks to 139.6 mA, so the access point is not pinned or limited at high current. This observation does not establish measurement accuracy or range behaviour at the 1.54 mA operating point.

Brief low-current excursions. The 30-minute off record contains exactly three events at 157.6 s, 158.9 s and 175.4 s, each 15 consecutive samples (0.15 ms) reading 0.2 µA. The same signature recurs once in the UART test, and 0.2 µA minima also appear in run 2. No other off-state sample falls below 1.33 mA. Their effect on the mean is about 0.0004 µA. The two excursions to about 0 nA noted in the September 2026 screenshot are consistent with the same signature. The cause of these excursions is unknown. An instrument artefact is possible, but the available evidence does not establish that explanation.

High-current events in run 2 (Figure 11). Analysis of the complete recording revealed events not visible on the application screen at the time: a spike to approximately 1.0 A at 20:40:32, followed by an uncommanded drop to the off-state level; two episodes reaching 1.68 A at 20:49:18 and 20:50:39; and a return to the on state at 20:50:51 without an operator-initiated power cycle. The operator attributed the high-current episodes to probe slips while measuring STATUS and VDD-EXT on the live header, but the specific pins bridged were not identified. The module answered AT commands afterwards. None of the results above is taken from the affected interval: the off-state figure is from run 3, recorded after the commanded power-down at 20:55:08, with no event above 1.82 mA. The off level reached after the uncommanded drop (1.539 mA) equals the level after the command.

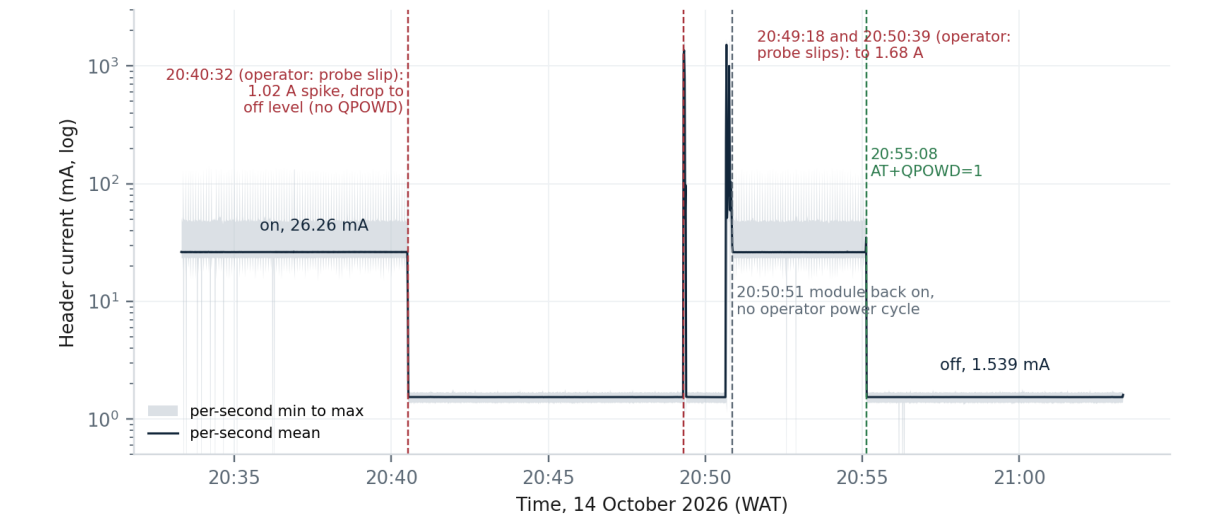


FIGURE 11 *DIP40CORE-A supply-header current during operation, high-current events and commanded power-down on 14 October 2026 (run 2).* Event annotations reflect the operator's account of probe slips; the pins bridged were not identified. The plot shows per-second mean current and the minimum-to-maximum range on a logarithmic scale. Times are in West Africa Time (WAT).

3.4 Comparison with the module specification

QUECTEL BG95 SERIES HD V1.5, TABLE 42 (3.8 V, ROOM TEMPERATURE; COLUMN "AVERAGE")	VALUE
Leakage: power-off, USB and UART disconnected	**12.99 µA**
PSM (Power Saving Mode)	3.89 µA
Rock Bottom: AT+CFUN=0 at sleep	0.575 mA
Sleep, LTE Cat M1, DRX = 1.28 s, USB disconnected	1.89 mA

The measured state is a confirmed power-off, so the like-for-like comparator is power-off leakage: **1.539 mA ÷ 12.99 µA ≈ 118.** Quectel's footnote to Table 42 states that PSM consumption is much lower than power-off, because more internal supplies are off and the internal clock runs slower. A PSM-state comparison against 3.89 µA would therefore be the stricter test.

3.5 Interpretation

The shared node leaves **two explanations consistent with the evidence**: **(a) board-level consumers** drawing current regardless of module state, or **(b) this module unit's own power-off draw** exceeding Quectel's family figure, which cannot be excluded because Quectel publishes no LA-variant figure.

Evidence of additional board-level current. Two resistive consumers sit permanently on the VBAT net: the U7 feedback divider, R26 15 kΩ + R27 3.9 kΩ to ground, which at 3.8 V draws 3.8 V ÷ 18.9 kΩ ≈ **0.20 mA** (from component values); and power LED D2 through R2 10 kΩ, about 0.1 to 0.2 mA depending on its unmeasured forward voltage. Together they account for roughly 0.3 to 0.4 mA of the 1.539 mA. These are **estimates from the drawing**: the board carries no reference designators, so R2 and R27 could not be located for a voltage reading.

The voltage measurements **support a third potential board-level current path**. U7's switch node is tied to VBAT through L3 while its input VIN is unconnected. With the module off and 3.8 V applied, VIN read **3.333 V** against VBAT 3.838 V: a drop of 0.505 V, close to the 0.518 V forward drop measured unpowered from VBAT to VIN in diode mode, and reversed polarity reading open. The VIN net is therefore back-powered from VBAT through a diode path, consistent with U7's high-side body diode (pre-set criterion: VIN ≥ 1.0 V supports the path; met). **How much current U7 and the VIN net draw in this condition is not measured**, and the JW5033H's quiescent current under back-feed has not been established. Resistor R7 (marked "0R/NC") would tie VBAT to the module's USB_VBUS pin if populated; its population could not be determined by inspection.

R1 and C21 are connected to PWRKEY. The vendor schematic and the BG95 40-pin DIP PCBA specification (note 7) place R1 (4.7 kΩ) and C21 (1 nF) on PWRKEY as part of the auto-start network. Neither component is in the VIN path or directly on VBAT. Their involvement in the module's return to the on state after the 20:50 supply disturbance (Figure 11) is plausible but was not established experimentally.

The deciding test is a header measurement in a network-confirmed PSM state, confirmed from the granted timers rather than inferred from current. It needs a live network and was not part of this assessment.

✗ **Engineering Finding** · Module-level current attribution is **not demonstrated** at the header of this board. The off-state header current, 1.539 mA, is about 118 times the module's published power-off leakage and reproduces the earlier record. The schematic identifies resistive consumers estimated at a fifth to a quarter of it, and the bench confirms a back-powered regulator input whose share is unmeasured; the remaining current has not been accounted for.

04

Cross-Board Comparison

ENGINEERING QUESTION

What do the two boards have in common, and what differs?

Two different questions can be asked of an off-state header reading. They use different comparators and must not be confused.

Question 1. Does the off-state header current exceed the module's own off-state specification? (Comparator: power-off figure.)

BOARD	HEADER CURRENT / TEST CONDITION	MODULE POWER-OFF FIGURE	STATISTIC	RATIO
BG95-M3 / DIP40CORE-A	1.539 mA; confirmed off (STATUS, VDD-EXT); 30 min mean	12.99 µA (Quectel V1.5, T42)	Average	**≈118×**
SIM7080G / Waveshare HAT	1.886 mA; powered down by PWRKEY, STA LED dark; 19.7 s mean, matching the 211.5 s level before power-on	15 µA (SIMCom V1.04, T6)	Maximum	**≥125×**

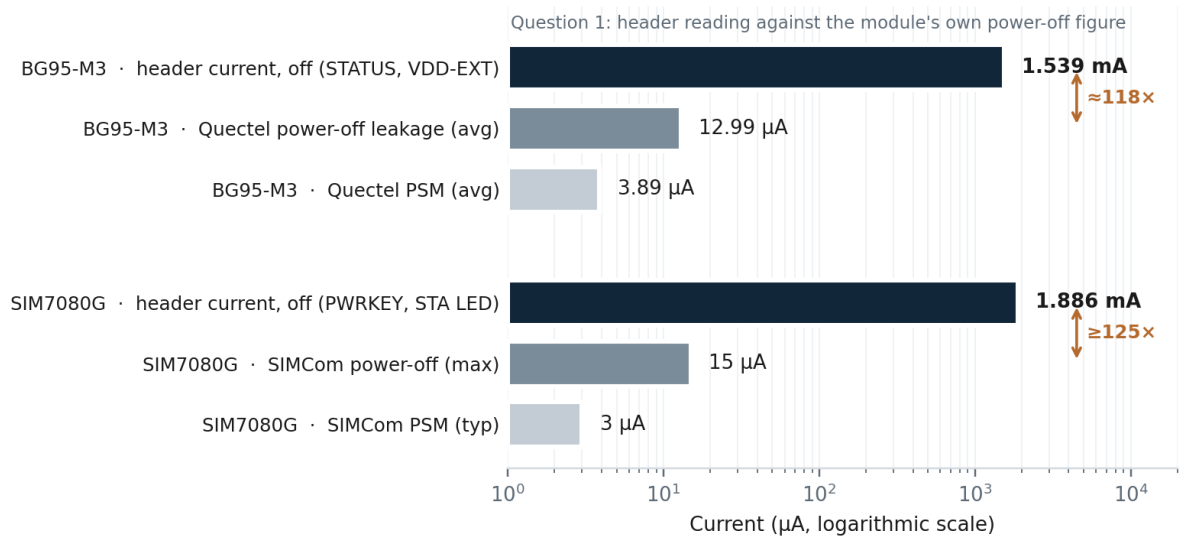


FIGURE 12 *Header current against module power-off specifications, both boards.* Logarithmic scale. The BG95-M3 power-off state was checked using STATUS and VDD-EXT; the SIM7080G was powered down through PWRKEY, with the STA LED dark in the off state and illuminated in the on state. STATUS voltage was not measured directly on the SIM7080G. Measured values: 14 October 2026 (BG95-M3) and 15 October 2026 (SIM7080G). Comparators: Quectel BG95 HD V1.5, Table 42; SIMCom SIM7080G HD V1.04, Table 6. The ratios use different reference statistics and should not be used to rank the boards.

Question 2. If the excess is board-level, can the module's power-saving current be resolved at this access point? (Comparator: the published PSM current.)

Illustrative comparison if the off-state baseline is board-level; PSM was not measured.

BOARD	OFF-STATE HEADER CURRENT	MODULE PSM FIGURE (PUBLISHED)	ILLUSTRATIVE RATIO
BG95-M3	1.539 mA	3.89 µA (Quectel V1.5, T42)	≈396×
SIM7080G	1.886 mA	3 µA typ. (SIMCom V1.04) · 3.2 µA (Waveshare)	≈629× · ≈589× (ERS-2026-002 published ≈687× and ≈644× from 2.06 mA)

	SIM7080G / WAVESHARE	BG95-M3 / DIP40CORE-A
Header topology	Shared VBAT net (vendor schematic)	Shared VBAT net (vendor schematic)
Off state established by	PWRKEY power-down; STA LED (driven by STATUS) dark when off, lit when on	STATUS and VDD-EXT pins, independent of current
Measurement record	Two 300 s recordings at 3.8 V, raw data retained; off-state windows 19.7 to 211.5 s. Earlier 10 s capture, supply unrecorded	30 min at 3.8 V, raw data retained, reproduced against an earlier 10 min record
Isolation of module contribution	PWR LED branch estimated at about 1.8 mA at 3.8 V, close to the whole baseline (not measured)	Partial: ~0.3 to 0.4 mA estimated from the drawing; regulator input back-powered (measured), share unmeasured; remainder unaccounted for
Attribution outcome	Not achieved	Not demonstrated

Combined findings. Two boards from different vendors, carrying modules from different manufacturers, each present a header current two orders of magnitude above the module's own power-off specification. These results do not establish a board fault. They show that the supply-header measurement includes board-level paths and does not isolate the module's current. Two boards are insufficient to determine how common this behaviour is.

Applicability to other operating states. If most of the off-state header current is due to board-level loads, that baseline would overwhelm the module's microamp-level power-off and PSM currents. In sleep and idle states, the published module currents are closer to the measured header baselines (SIMCom sleep 1.2 mA against 1.886 mA; Quectel Cat M1 sleep 1.89 mA and Rock Bottom 0.575 mA against 1.539 mA), so a header reading would represent a mixture of module and board consumption. If board and module currents add, and treating each baseline as board-level (not established for either board), the board would be about 61 % of a SIMCom sleep reading (1.886 of 3.086 mA), about 45 % of a Quectel Cat M1 sleep reading (1.539 of 3.43 mA) and 73 % of Rock Bottom (1.539 of 2.11 mA). In two of the three comparisons, the estimated board contribution is larger than the module contribution.

Limitations of the findings. The results do not establish that all carrier boards behave this way, or how large the excess will be on any other board. The two boards support a measurement procedure but do not establish how prevalent this behaviour is. The comparators are different statistics, the off-state windows differ (30 minutes against 20 seconds to 3.5 minutes), and the isolation quality differs.

■ **Engineering Finding** · On both boards, a header reading taken as module power-off current would have described the board, or at best an unresolved mixture of board and module, at about two orders of magnitude above the module's own figure. If the excess is board-level, the same baseline would also mask the module's PSM current; PSM was not measured.

05

Procedure: What a Header Reading Measures

ENGINEERING QUESTION

What should an engineer do before treating a carrier-board header reading as module current?

The procedure below reflects the steps used to evaluate both boards and the failure modes observed during measurement. On the Waveshare HAT re-measurement, step 4 rests on PWRKEY control and the STA LED rather than a metered STATUS reading, the step 5 off-state windows are shorter than 10 minutes, and step 6 did not apply because no interface lines were connected.

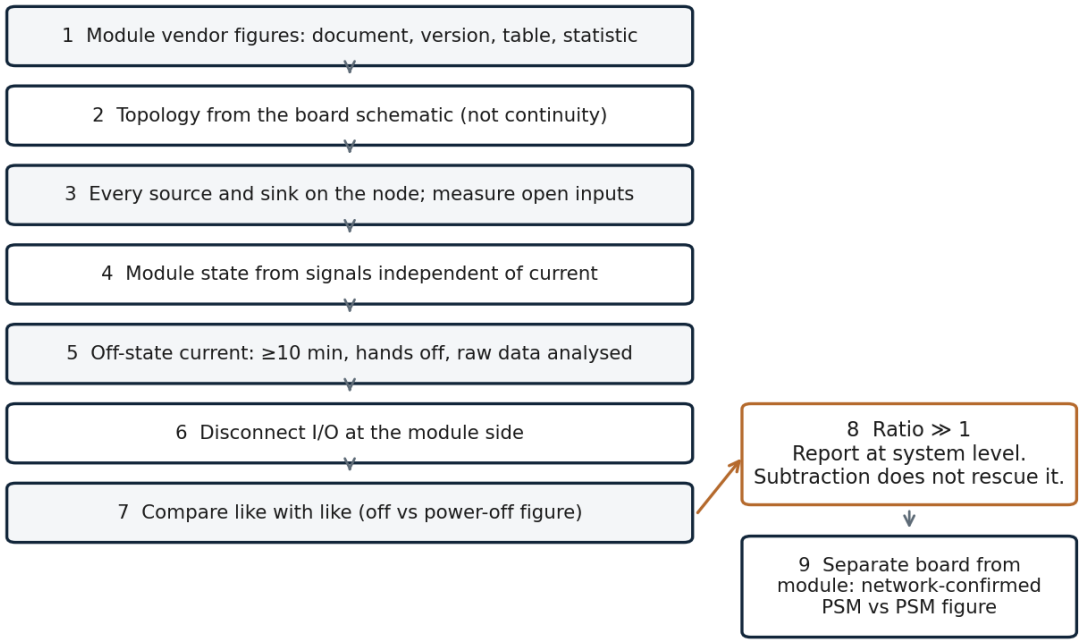


FIGURE 13 *Header-attribution procedure.* Decision flow of the steps tabulated below. Derived from §§02 to 04.

STEP	ACTION	PITFALL ENCOUNTERED
1	Obtain the module manufacturer's hardware design document; record version, table and statistic for power-off, PSM and sleep	Table numbers shift between revisions (SIMCom: Table 31 in V1.03, Table 33 in V1.04); a board vendor's restatement can differ from the module vendor's figure (3.2 µA against 3 µA)
2	Establish supply topology from the board schematic, not from a pin-assignment sheet	**A continuity check cannot distinguish a series tap from a parallel one**; both read as continuous. Boards without reference designators cannot be probed component by component
3	On a shared node, identify every other source or sink. Leave unused supply inputs open, then **measure them**: an open input can be back-powered from the rail	An unconnected regulator input read 3.33 V, fed from VBAT through a diode path

STEP	ACTION	PITFALL ENCOUNTERED
4	Establish module state from signals independent of current, before and after the state change	**Never label a state from its own current reading.** Indicator behaviour differed between sessions (POWERED DOWN response); STATUS off read at the criterion limit, so a second signal (VDD-EXT) was needed. AT+CFUN=0 gates RF, not baseband
5	Measure off-state header current with a validated instrument, at the specified supply voltage, over at least 10 minutes, hands off, and save the raw data. **Analyse the raw file, not the screen**	Static screen captures did not reveal an uncommanded drop to the off-state level or two events reaching 1.68 A. Analysis of the complete recording identified these events. The operator attributed the high-current episodes to probe slips, but the pins bridged were not identified. Record and inspect the full sequence; size the recording for the whole sequence; guard the current for the whole session, not only at power-up
6	Remove interface back-feed by disconnecting I/O at the module side, during a recording	Host-side disconnection does not exclude injection beyond a level-shifting network
7	Compare like with like: off-state reading against off-state figure, same statistic where possible	None
8	If the ratio is much greater than one, attribution is not available here; report at system level	**Subtraction does not rescue it**: valid only for a static baseline, while board load varies with supply droop during dynamic events (ERS-2026-002 §04)
9	To separate board from module, confirm PSM from network-granted timers and measure in that state	The PSM figure is the stricter comparator

Probing a live header. Measuring module pins on an energized board risks bridging adjacent pins; on this board VBAT (39) sits beside GND (40). Count pins visually or with the supply off, use a clip on the ground lead, and keep the current under continuous watch while probing.

Scope of Evaluation

THIS ASSESSMENT EVALUATES	THIS ASSESSMENT DOES NOT EVALUATE
Off-state current at the supply header of two carrier boards	Sleep, PSM or eDRX current under a live network
Supply topology from vendor documentation	Any board other than the two evaluated
Independent establishment of module power state (both boards)	Statistical behaviour across multiple units of either module
UART back-feed test by a recorded module-side disconnection (DIP40CORE-A)	The share of each board-level consumer (both boards)
A candidate board-level path by measurement (DIP40CORE-A: back-powered regulator input)	Any modified board; any energy consumption result
A procedure for deciding header attribution	Temperature dependence. Ambient 27 °C at the start (15:36 WAT) and end of the 14 October bench session (SHT30 sensor, calibration unknown), not logged continuously during the 20:22 to 22:37 measurements; not recorded on 15 October

A DECLARED LIMITATION

On the DIP40CORE-A the cause of the excess is unresolved between board-level consumers and this module unit. The deciding test, a header measurement in network-confirmed PSM, needs a live network and was not performed.

The DIP40CORE-A is therefore graded "not demonstrated": the excess may be board-level, but module draw above Quectel's figure has not been excluded.

Engineering Evidence Summary

ENGINEERING CRITERION	OUTCOME
Measurement chain fitness	■ **Qualified** agreement within 0.6 % at three check points, two of them against nominal-value calculations and one against a calibrated reference (ampere mode, 470 mA); off-state operating points (source meter, 1.5 to 1.9 mA) not checked
Waveshare HAT off-state attribution	✗ **Not achieved** ≥125× module power-off maximum at 3.8 V; evidence points to board-level consumption
Waveshare HAT module state	✓ **Established** PWRKEY power-down; STA LED dark when off, lit when on
Waveshare HAT off-state repeatability	✓ **Within 0.6 %** before power-on and after power-down, both recordings
DIP40CORE-A off-state current reproduced	✓ **Met pre-set criterion** 1.539 mA over 30 min against 1.53 mA ± 5 %; raw data retained
DIP40CORE-A module state, independently established	✓ **Established** STATUS 1.8 V / 0.45 V (off at the limit); VDD-EXT 1.81 V / 0.000 V
DIP40CORE-A UART back-feed	✓ Module-side UART disconnection changed mean header current by less than 0.13 %, below the pre-set 2 % exclusion threshold
DIP40CORE-A regulator-input back-power	■ **Back-power path supported**; current contribution unmeasured. VIN = 3.333 V; VBAT = 3.838 V
DIP40CORE-A off-state attribution	✗ **Not demonstrated** ≈118× module power-off leakage; cause unresolved
Header-attribution procedure	✓ **Defined** §05

Radianode Engineering Position

Following independent engineering evaluation, Radianode considers that **a supply-header reading on an off-the-shelf cellular carrier board should not be reported as module current** unless the following conditions are met and recorded.

#	OPERATING CONDITION
1	**The off-state header current has been measured and compared, like for like, with the module manufacturer's published off-state figure**, cited by document version and table
2	**Module state was established independently of the current reading**
3	**Results are labelled at the attribution level they support.** System-level results are not presented as module-level results

Module-level attribution requires a board that exposes the module supply in series, or a modification that this assessment's constraint excludes. On the DIP40CORE-A, the network-confirmed PSM comparison is recommended before any statement is made about where the excess current originates.

ENGINEERING READINESS OUTCOME

MODULE-LEVEL OFF-STATE CURRENT NOT ATTRIBUTABLE AT THE SUPPLY HEADER OF EITHER BOARD

System-level header-current measurements remain available on both boards
Next step: DIP40CORE-A header measurement in network-confirmed PSM

Appendix A: Figure Traceability

REPORT FIGURE	ENGINEERING WORKFLOW	SOURCE EVIDENCE
Figure 1: PPK2 operating mode	Measurement basis	Instrument screenshots, 14 October and September 2026
Figure 2: Waveshare HAT header current	Carrier board current assessment	Raw sample data, 15 October and 26 August 2026
Figure 3: Waveshare HAT baseline (reproduced)	ERS-2026-002	ERS-2026-002 Figure 4
Figure 4: Waveshare HAT measurement configuration	Competing-source check; module state	Board photographs, 26 August and 15 October 2026
Figure 5: Waveshare HAT VBAT net (redrawn)	Topology assessment	Waveshare HAT schematic
Figure 6: DIP40CORE-A module (BG95-M3)	Identity	Marking photograph, 14 October 2026
Figure 7: DIP40CORE-A VBAT net (redrawn)	Topology assessment	DIP40CORE-A schematic; bench measurements, 14 October 2026
Figure 8: DIP40CORE-A connections	Competing-source check	Bench session record, 14 October 2026
Figure 9: DIP40CORE-A off-state current, 30 min	Physical attribution baseline	Raw sample data, 30-minute off-state recording
Figure 10: UART disconnection test	Back-feed test	Raw sample data, UART disconnection test
Figure 11: DIP40CORE-A current, operation to power-down	Session record	Saved instrument recording, 14 October 2026
Figure 12: Both boards vs specifications	Cross-board comparison	Raw sample data, both boards; Quectel and SIMCom hardware design documents
Figure 13: Procedure	Procedure definition	§§02 to 05

Source files and their SHA-256 hashes are listed in the companion ERS-2026-003 Reproducibility Statement.

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